VALPARAISO UNIVERSITY

COMPUTING AND INFORMATION SCIENCES

Parallella

Background

This system is a computing cluster that was assembled at the University as part of an ongoing interdisciplinary faculty/student project to enhance the facilities and teaching of parallel computation across multiple classes. It provides a hands-on, small form factor platform for illustrating a variety of topics, and is a working illustration of several ongoing trends in computing. These include low-power consumption technologies, post-manufacturing reconfigurable circuitry (FPGAs), reduced instruction set computing (RISC), and the flexibility and utility of multicore consumer/commodity grade devices.

Technical Specifications

- Processing (5 nodes):
  - One 16-core RISC SOC per node
  - 2 Zynq SOC (FPGA + ARM9) per node
- Interconnect: Gigabit Ethernet
- Power: 5W per node
  (cluster runs on 1 standard outlet)
- RAM: 1 GB SDRAM per node
- Storage: X GB MicroSD storage/node
- Operating System: Linux
- Cooling: 2x external fans

Curricular Use

- (planned) Parallel and Distributed Computing Elective (Graduate and Undergraduate levels)
- (planned/as time permits) Data structures topics in CS 158
- (as requested) Courses in Electrical and Computer Engineering

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